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Replacing obsolete processors

MEMS as well as the Institute of Microelectronics occasionally receive inquiries for a chip replacement. This happens mostly due to the fact, that devices like microcontrollers used and manufactured decades ago, today happen to be obsolete. Reengineering assembler source code to get the same behavior is a big investment in time. So the purpose of the collaboration was to find an efficient way to improve chip replacement techniques by reengineering the core including interfaces on an FPGA platform.

Common open source IP cores can be found online. As for example for the famous MC6800 microcontroller, the open core ao68000 can be downloaded. The problem with those IP cores is that they do not support the original interface to access external peripherals; instead they use on-chip interfaces like Wishbone.

Reengineering a bus interface based on an old chip technology, with a modern FPGA, generates issues concerning I/O timing. As modern chip technologies are much faster, problems like setup and hold timing violations can occur. Developing a method to reproduce exact I/O timings was the main part of the project.

A complete processor re-engineering introduces complex tasks. Datasheets cover the instruction set architecture (ISA) but not the explicit microarchitecture which describes the way a given ISA is implemented in a processor. Therefore a verification concept to examine timing similarity to the original microcontroller was further elaborated.

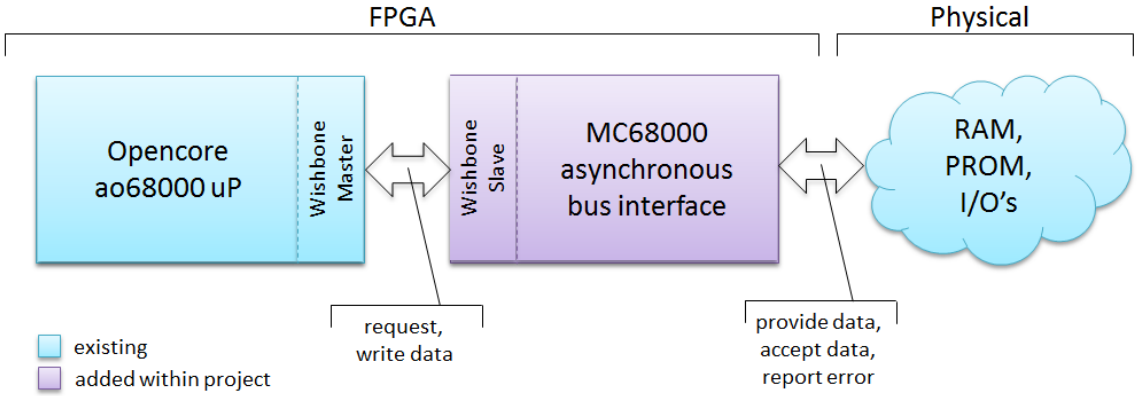
Collaboration

MEMS AG initiated and leaded this project. Please contact us for questions on this subject.

The Aargau Research Fund supported this project to encourage innovative projects in economics for canton Aargau.

The Institute of Microelectronics (IME) is the center of excellence for microelectronics which supervised this project with Professors in FPGA design.

A Master student in the MSE degree course developed the strategy and method to replace obsolete processors with FPGA as one of his projects.



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